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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

KANG, DONGHEE

ART UNIT PAPER NUMBER

2811

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/666,325

Applicant(s)

ARMBRUST ET AL.

Examiner

Donghee Kang

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2002.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 15-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Remarks*

1. Applicant's Amendment and Response to Paper No.17 has been entered and made of Record.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **15-34** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims **15, 21, & 29**, the phrase "*a thickness* of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicide surface" is unclear because the thickness is not defined by the claim.

Claims **21 & 29** recite the limitation "a thickness of *said uppermost layer*" in lines 5 & 7, respectfully. There is insufficient antecedent basis for limitation "*said uppermost layer*".

Claims **16-20, 22-28 & 30-34** are rejected since each includes the limitations of independent claims 15, 21 & 29.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims **15-18, 21-24, & 27-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ngo et al. (US 6,303,505).

Regarding claims **15 & 16**, Ngo et al. teaches a semiconductor device comprising (Fig.5):

A first level of substantially silicide free metallurgy (12); an uppermost layer of metallurgy comprising copper (13A), wherein a top of said uppermost layer comprises a silicide layer (30).

Ngo et al. does not expressly teach the copper interconnection layer for a bonding pad. However, it is known fact that an increase in circuit density corresponds to a decrease in conductor dimensions, which leads to higher resistance and current densities, which increases the signal losses and promote electromigration damage to the conductors on the electronic devices and packages. These problems can be solved using a copper interconnection layer because of it's good electrical conductivity as known in the art. Therefore, it would have been obvious in the art at the time the invention was made to use the copper interconnect layer as a bonding pad in IC device, since the copper interconnect layer has a good electrical conductivity.

Ngo et al. does not expressly teach a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicide layer. However, it is inherent that a thickness of said uppermost layer taught by Ngo et al. will reduce sensitivity to resistivity shifts associated with said silicide layer since a structure of Ngo's device is identical with the claimed structure.

Regarding claim **17**, Ngo et al. teaches the method of cleaning of uppermost layer by applying a hydrogen-containing plasma prior to formation of silicide surface (Col.5, line 60 - Col.6, line8).

Regarding claims **18, 21-22 & 27-30**, Ngo et al. teaches a semiconductor device comprising (Fig.5):

an exterior surface having a top level of metallurgy (13A); and an interior having at one internal level of metallurgy (12), wherein said top level of metallurgy is thicker than said internal level of metallurgy, wherein the top level of metallurgy comprises a silicide layer (40), wherein said top level of metallurgy comprises copper.

Ngo et al. does not expressly teach the copper interconnection layer for a bonding pad. However, it would have been obvious for the same reason as given for the rejection of claim 15 (see above).

Ngo et al. does not expressly teach the copper silicide layer comprises 10% to 20% of a thickness of the top level of metallurgy. However, Ngo et al. teaches a copper silicide layer has a thickness of about 10Å to about 1000Å, which is in the inventive thickness ranges where the thickness of silicide layer is approximately 1000Å in this application (page 8, line 21). Therefore, the copper silicide layer of Ngo would have a 10% to 20% of a thickness of the top level of metallurgy since both silicide layers have a same thickness.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Ngo et al. does not expressly teach a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicide layer. However, this feature is inherent because a structure of Ngo's device is identical with the claimed structure.

Regarding claims **23-24 & 31-32**, Ngo et al. teaches the method of cleaning of top level of metallurgy by applying a hydrogen-containing plasma prior to formation of silicide surface (Col.5, line 60 - Col.6, line8) to make top level of metallurgy is free of oxides and silicide islands.

6. Claims **19-20, 25-26 & 33-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ngo et al. in view of Ohashi et al. (US 6,184,143).

Ngo et al. teaches the semiconductor device further comprises a silicon nitride layer (50) physically connected to said silicide surface. Ngo et al. does not expressly teach silicon nitride layer including an opening allowing direct electrical contact with solder terminal. However, Ohashi et al. teaches in Fig.76 solder terminal (136) directly connected to copper bonding pad (M5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solder terminal on the copper interconnection of Ngo, which includes silicide surface, in order to facilitate electrical connection of the semiconductor structure with an external connector, such as modulator package substrate.

7. Claims **15-18, 21-24 & 27-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Filipiak et al. (US 5,447,887).

Regarding claims **15-16**, Filipiak et al. teaches a semiconductor device comprising (Fig.5):

Art Unit: 2811

A first level of silicide free metallurgy (26); an uppermost layer of metallurgy (30), wherein a top of said uppermost layer comprises a silicide layer (32); and a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicide layer.

Filipiak et al. does not expressly teach the copper interconnection layer for a bonding pad. It would have been obvious for the same reason as given for the rejection of claim 15.

Regarding claims 17, 23-24 & 31-32, Filipiak et al. does not teach the method of cleaning of uppermost layer by applying a hydrogen-containing plasma prior to formation of silicide surface (Col.5, line 60 - Col.6, line8). This is a product-by-process limitation. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production.

If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process". In re Thorpe, 777F. 2d 695,698 USPQ 964, 966 (Fed. Cir.1985). See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claim 18, Filipiak et al. does not teach the silicide surface comprises a top 10% to 20% of a thickness of said uppermost layer. However, Filipiak et al. mentioned that the thickness of silicide can be changed depending on the application of device (Col.5, line 63 – Col.6, line 6). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that where the

Art Unit: 2811

general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims **21-22, 27-28 & 29-30**, Filipiak et al. teaches a semiconductor device comprising (Fig.5):

An exterior surface having a top level of metallurgy; an interior having at least one internal level of metallurgy, wherein said top level of metallurgy is thicker than said internal level of metallurgy,

wherein the exterior surface comprises a silicide layer,

wherein said top level of metallurgy comprises copper; and a thickness of said uppermost layer reduces sensitivity to resistivity shifts associated with said silicide layer.

Filipiak et al. does not expressly teach the copper interconnection layer for a bonding pad. It would have been obvious for the same reason as given for the rejection of claim 15.

Filipiak et al. does not teach the silicide thickness which is in the ranges 10% to 20% of the total thickness of the copper interconnect layer. However, Filipiak et al. mentioned the thickness of silicide layer can be changed depend on the application of device (Col.5, line 63 – Col.6, line 6). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

8. Claims **19-20, 25-26 & 33-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Filipiak et al. in view of Dass et al. US 6,046,101).

Filipiak et al. does not teach the semiconductor device further comprises a silicon nitride layer (34) physically connected to said silicide layer and a solder terminal electrically connected to bonding pad. However, Dass et al. teaches in Fig.21 the solder terminal (270) connected to bonding pad and a silicon nitride (245). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the solder terminal in order to facilitate electrical connection of the semiconductor structure with an external connector, such as modulator package substrate.

### ***Response to Arguments***

9. Applicant's arguments filed September 5, 2002 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 15-34 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that it has not been shown where Filipiak et al. teaches or suggests the 10% - 20% of the copper layer is the silicide layer. These matters have been pointed out in the statement of rejection in the paragraph above with respect to claims 18, 21 & 29.

Filipiak et al. teaches silicidation thickness can be changed (Col.6, lines 1-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the thickness of silicide layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

### ***Conclusion***

Art Unit: 2811

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



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DHK  
November 13, 2002